Double Patterning Combined with Shrink Technique to Extend ArF Lithography for Contact Holes to 22nm Node and Beyond

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Abstract

Lithography becomes much more challenging when CD shrinks to 22nm nodes. Since EUV is not ready, double patterning combined with Resolution Enhancement Technology (RET) such as shrink techniques seems to be the most possible solution. Companies such as TSMC[1] and IBM[2] etc. are pushing out EUV to extend immersion ArF lithography to 32nm/22nm nodes.

Last year, we presented our development work on 32nm node contact (50nm hole at 100nm pitch) using dry ArF lithography by double patterning with SAFIER shrink process[3]. To continue the work, we further extend our dry lithography capability towards the 22nm node. We demonstrated double patterning capability of 40nm holes at 80nm pitch using ASML XT1400E scanner. It seems difficult to print pitches below 140nm on dry scanner in single exposure which is transferred into 70nm pitch with double patterning.

To push the resolution to 22nm node and beyond, we developed ArF immersion process on ASML XT1700i-P system at the College of Nanoscale Science and Engineering (Albany, NY) combined with a SAFIER process. We achieved single exposure process capability of 25nm holes at 128nm pitch after shrink. It enables us to print ~25nm holes at pitch of 64nm with double patterning.

Two types of hard mask (HM), i.e. TIN and a-Si were used in both dry and immersion ArF DP processes. The double patterning process consists of two HM litho-shrink-etch steps. The dense feature is designed into two complementary parts on two masks such that the density is reduced by half and minimum pitch is increased by at least a factor of \(2^{1/2}\) depending on design. The complete pattern is formed after the two HM litho-shrink-etch steps are finished.

Keywords: double patterning, immersion, ArF lithography, RET, SAFIER, Shrink, Hard Mask

1. INTRODUCTION

The semiconductor industry is being driven by “Moore’s law” towards smaller feature sizes and pitches. Contact holes for technology node of 32nm and below are extremely difficult using ArF lithography. EUV is expected to be the candidate for 32nm and 22nm node. Since it is not ready, double patterning has become the most possible solution to achieve minimum half pitch of 50nm and below. We continue our double patterning work to explore the best possible resolution using both dry and immersion ArF lithography.

In the study of dry ArF process, a 300nm lithography system at Applied Material consists of ASML XT1400E and a Sokudo RF3 track, and Brewer Science BARC ARC29A, TOK ArF resist TARFP7070 were used. SAFIER process is applied to shrink the holes and improve resist profile.

The double patterning process consists of a 1st hard mask (HM) litho and shrink, follow by 1st HM etch, resist strip and clean. Next are the 2nd HM litho and shrink, followed by a 2nd HM etch, resist strip and clean. Two HM schemes are developed for the double patterning process. The 1st HM scheme used thin layer of TIN and the 2nd HM used a-Si for
lithography patterning. The dry ArF processes in both schemes were evaluated. It demonstrated the capability of 40nm half pitch contact hole patterning.

To further improve resolution, a study of ArF immersion lithography combined with SAFIER shrink was carried out. We established process condition for SAFIER with immersion resist. Working with the College of Nanoscale Science and Engineering (CNSE), on an ASML XT1700i-P, we were able to print contact holes of ~25nm at 64nm pitch using double patterning technique. Similar double patterning steps as mentioned in the ArF dry lithography were applied to the immersion ArF DP process. We printed wafers at the CNSE using JSR top coat TCX041, Rohm Haas resist EPIC2135, and AZ ArF18B BARC. The wafers were then processed through SAFIER shrink and etch at Applied Materials.

2. DOUBLE PATTERNING DRY ARF LITHOGRAPHY PROCESS DEVELOPMENT

Because of non-availability of EUV system, the industry has been actively evaluating and developing double patterning schemes to enhance resolution to meet the demand of 32 and 22nm technology node. Our double patterning processes are developed based on two hard mask schemes that can be used for both FEOL and BEOL. Double SAFIER steps are used to shrink holes, improve their profile and circularity.

Depth of focus is characterized to check the process window. DICD data are collected after double SAFIER process. Figure 1 plots the DOF from the focus exposure matrix (FEM) wafer printed on ASML XT1400EX. The DOF is about 0.12 micron for contact holes of 45nm. When the hole size is larger than 50nm, DOF is more than 0.15 micron. Figure 2 shows top down SEM images of 45nm contact holes through focus from -0.03 to 0.09 micron.

In Figure 3, we plot CD data for 40 and 50nm contact holes of 10 wafers after HM litho & shrink and HM etch. The DICD 3σ is less than 5nm. While FICD 3σ is less than 8nm with majority under 6nm. The data indicate good uniformity of 40 and 50nm contact holes.

Fig. 1. DOF curves of contact hole at different exposure energy. ASML XT1400EX. Illumination condition: Annular, NA = 0.85, Sigma = 0.85/0.55.

Fig. 2. Top down SEM images of 45nm contact hole at defocus positions. Verity SEM, FOV: 1.5
Figure 3. Left charts plot the contact DICD and FICD trend in the lot. Right charts show the CD uniformity after HM litho and etch. ASML XT1400EX for litho and AMAT AdvantEdge etcher.

Figure 4 shows the schematic diagrams that illustrate the double patterning process steps after 1\textsuperscript{st} HM litho & shrink, 1\textsuperscript{st} HM etch, 2\textsuperscript{nd} HM litho & shrink, and 2\textsuperscript{nd} HM etch, respectively. The top down SEM images in Figure 5 are the actual wafer images of 45nm features at pitch of 90nm after 1\textsuperscript{st} TIN HM litho & shrink, 1\textsuperscript{st} TIN HM etch, 2\textsuperscript{nd} HM litho & shrink, as well as 2\textsuperscript{nd} HM etch, respectively. In the 2\textsuperscript{nd} HM litho process, different X and Y shift can be applied to get different post double patterning features as shown in Figure 5.

To print contact holes with smaller pitch, different illumination conditions were used. The top down SEM image at left in Figure 6 shows 40nm holes at pitch of 73nm. The patterns were formed at pitch of 146nm in single exposure which is near the best resolution that we may get from dry ArF lithography scanner system - ASML XT1400EX \cite{4}. The SEM image at right of Figure 6 shows the 40nm holes at pitch of 80nm. The process condition for 40nm half-pitch (HP) is similar to those of 45nm HP as discussed above which is manufacturable with reasonable process window for double patterning using dry ArF lithography. The CD uniformity is stable as indicated in Fig. 3.

![Fig. 3. Left charts plot the contact DICD and FICD trend in the lot. Right charts show the CD uniformity after HM litho and etch. ASML XT1400EX for litho and AMAT AdvantEdge etcher.](image1)

![Fig. 4. Schematic diagram for contact HM double pattering flow.](image2)

![Fig. 5. Top down SEM images of 45nm features after 1\textsuperscript{st} TIN HM litho & shrink, 1\textsuperscript{st} TIN HM etch, 2\textsuperscript{nd} HM litho & shrink, and 2\textsuperscript{nd} HM etch.](image3)

![Fig. 6. Top down SEM images of 40nm holes at pitch of 73nm and 80nm.](image4)
As mentioned earlier, two types of HM were used in the double patterning study. TIN and a-Si were selected because they have good contrast. At the 2nd litho step, different shifts were applied to the wafers for structures of 200nm, 180nm, and 160nm pitches. Therefore, after double patterning, we were able to obtain contact holes of 50nm at 100nm pitch, 45nm at pitch of 90nm, and 40nm at 80nm pitch, respectively. SEM images in Figure 7 show the hole profile using TIN and a–Si HMs at 50, 45, and 40nm half pitch. It is seen that Both TIN and a-Si were served well as HM in the double patterning schemes.

Based on our experiments, 40nm half pitch seems to be the most reasonable resolution from dry ArF double patterning process.
Immersion ArF process combined with SAFIER was developed to further improve the resolution and process window. We have used a-Si HM in the immersion process development. Figure 8 plots DOF curves of contact hole at 130nm pitch from a FEM wafer printed on the ASML XT1700i-P. The DOF is \( \geq 0.15 \) micron for holes \( \geq 55 \)nm, which is considered sufficient enough for manufacturing.

To improve the hole circularity and profile, various SAFIER conditions were studied. When SAFIER bake temperature is below 160 \( \degree C \), shrinkage is not significant. While bake temperature is above 180 \( \degree C \), holes are damaged. It is found that SAFIER bake temperature from 160 to 170 \( \degree C \) is suitable for the resist. In the study, SAFIER bake temperature of 168 \( \degree C \) was selected. Figure 9 shows the 25nm holes with good profile after SAFIER shrink. DOF curves of contact hole at 130nm pitch before and after SAFIER shrink are plotted in Figure 10. It can be seen that DOF remains the same after SAFIER process. For 30nm holes, DOF is about 0.18 micron at 130nm pitch. Figure 11 shows the SEM images of contact holes of 130nm pitch through focus before and after SAFIER.

It is very challenging to etch holes smaller than 25nm. After etch, the holes look not as clean as compared to those holes with larger sizes from dry ArF DP process. Some residues were observed and difficult to remove with wet clean, even after multiple attempts to test various etch chemistry options. Therefore, we determined to target at 25 to 30nm at pitch of 64nm (for 32nm HP). Figure 12 illustrates the double patterning images after 1st HM litho \& shrink, 1st HM etch, 2nd HM litho \& shrink, as well as 2nd HM etch, respectively.

Experimental studies show that contact etch FICD depends largely upon the etch process of BARC step. The contact CD defined by BARC step will be transferred to a-Si HM layer below, and further into USG and APF layers. It’s critical to avoid CD blow-up, or even being able to shrink CD in contact hole after BARC step. There are three main chemistries that are usually used to etch BARC: CF4-based, Cl2-based and HBr-based. HBr-based BARC process is typically used.
in gate etch application where poly line trimming after BARC open is required. That’s because this process will cause line CD loss, and it means space CD gain. Thus HBr-based BARC process is not good candidate for small contact hole etch, as it will result in CD blow-up. In order to compare CF4 and Cl2 based BARC processes, we did extensive experiments by tuning gas ratio, bias power and pressure. We found out that although we can get similar FICD after BARC step using either chemistry, the CF4-based BARC step always gave us larger FICD after Si etch step, even we use same Si etch process after BARC open. One possible explanation is that there are some F-based residues left on wafer surface after CF4-based BARC step, and these F-based residues will continuously attack the sidewall and bottom of a-Si contact hole, which caused the FICD blow-up. After taking all these results into consideration, we finalized the etch process with BARC open (Cl2/O2), Si ME (Cl2/HBr/O2), Si SL (HBr/O2) and Si OE (HBr/O2) etch steps, and the top view SEM images after etch are shown in Fig 12.

Although resist CD of 25nm is obtained, which meets the requirement of 20nm node per IRTS roadmap, it seems difficult to etch such small patterns. The etch process is still under tuning to improve etch profile and uniformity. The hard mask scheme directly associated with etch process and etch pattern profile may need further study based on litho and etch process capability with consideration of integration requirement. More work will be continued.

Fig. 8. DOF curves of contact hole at 130nm pitch. ASML XT1700i-P. NA = 1.2, Quasar 30, Sigma O/I = 0.92/0.75.

Fig. 9. Immersion ArF resolution capability with single exposure and SAFIER process, 25nm hole at pitch of 130nm at different magnifications (FOV: 1.5 for left image and 0.75 for right image). ASML XT1700i-P.
Fig. 10. Depth of focus of contact holes before and after a 168 °C SAFIER process. ASML XT1700i-P.

Fig. 11. Top down SEM images at defocus positions. Top and bottom row are images before and after SAFIER process, respectively. FOV: 1.5.

Fig. 12. Top down SEM images illustrate the contact holes using a-Si HM after 1st HM litho, 1st HM etch, 2nd HM litho and etch, respectively. CD = 25nm at pitch of 64nm. FOV: 0.75
4. CONCLUSIONS

We have developed the double patterning process using both dry and immersion ArF lithography processes combined with SAFIER shrink. We evaluated DP processes based on two hard marks schemes, i.e. TIN and a-Si. We successfully achieved the resolution of 40nm at pitch of 80nm using dry ArF DP process. We demonstrated printability of 25nm contact holes at pitch of 64nm using immersion DP process. Etching small holes for 22nm node and below is very challenging and needs more effort in the development.

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6. REFERENCES