Interactions of double patterning technology with wafer processing, OPC and design flows

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ABSTRACT

Double patterning technology (DPT) is one of the main options for printing logic devices with half-pitch less than 45nm; and flash and DRAM memory devices with half-pitch less than 40nm. DPT methods decompose the original design intent into two individual masking layers which are each patterned using single exposures and existing 193nm lithography tools. The results of the individual patterning layers combine to re-create the design intent pattern on the wafer. In this paper we study interactions of DPT with lithography, masks synthesis and physical design flows. Double exposure and etch patterning steps create complexity for both process and design flows. DPT decomposition is a critical software step which will be performed in physical design and also in mask synthesis. Decomposition includes cutting (splitting) of original design intent polygons into multiple polygons where required; and coloring of the resulting polygons. We evaluate the ability to meet key physical design goals such as: reduce circuit area; minimize rework; ensure DPT compliance; guarantee patterning robustness on individual layer targets; ensure symmetric wafer results; and create uniform wafer density for the individual patterning layers.

Keywords: double patterning technology (DPT), standard cell design, place & route, design rules.

1. Introduction and background

Double patterning technology (DPT) is one of the main options for printing logic devices with half-pitch less than 45nm; and flash and DRAM memory devices with half-pitch less than 40nm [1, 2]. DPT methods decompose the original design intent into two individual masking layers which are each patterned using single exposures and existing 193nm lithography tools. The results of the individual patterning layers combine to re-create the design intent pattern on the wafer. As there are different DPT methods being discussed in the industry, in this paper we define DPT as a pitch-splitting method with a patterning sequence litho1-etch1-litho2-etch2 [1], see Figure 1. For the 22nm logic node likely DPT layers are contact and metal1, possible layers include poly, active, viax and metalx.

DPT will have several interactions with the mask synthesis and physical design areas. DPT decomposition is a critical software step which will be performed in physical design (to ensure DPT compliance of the layout) and also in mask synthesis (to create the individual patterning layer wafer targets). Decomposition includes cutting (splitting) of original design intent polygons into multiple polygons where required; and coloring of the resulting polygons (i.e., deciding which individual masking layer each polygon will be placed on). Key physical design goals are to reduce circuit area; minimize rework; ensure DPT compliance; guarantee patterning robustness on individual layer targets; ensure symmetric wafer results; and create uniform wafer density for the individual patterning layers. In this paper we study interactions of
DPT with lithography, masks synthesis and physical design flows. All DPT decomposition was performed using Proteus™, standard cells were created using Cadabra™, litho simulations were performed using Sentaurus Lithography™, and metal routing was created using IC Compiler™.

2. Lithography implications of double patterning

One important interaction between lithography processing and double patterning is the need for single exposure patterning in DPT to create semi-isolated features very accurately. Figure 2 shows an example of a very dense 1:1 line:space ratio final DPT etched pattern which is composed of two individual patterns, each having a semi-isolated 1:3 line:space ratio. Each individual 1:3 line:space pattern must be created with excellent focus stability. However, it is well known that semi-isolated patterns have inherently poor aerial image focus stability. RET methods are often employed to enhance depth of focus (DOF), but methods such as addition of sub-resolution assist features (SrAFs) or upsizing of the final wafer pattern (retargeting) cannot be employed here due to insufficient spacing between features. Two non-RET methods which can be employed to improve DOF of semi-isolated features are chemical diffusion shrink of the aerial image during the creation of the resist image (e.g., acid or base diffusion in the resist), and the combination of lithography CD upsizing followed by an etch CD shrink technique (such as trim etch for lines or tapered profile etch for trenches/vias). Both of these RET methods essentially enable the aerial image to be created at approximately a 50% local pattern density (e.g., 1:1 line:space or 1:1 trench:space) for high DOF, but with the final wafer pattern shrink down to the required 1:3 ratio. Resist trim etches and chemical diffusion CD shrink are typical for active, poly gate and contact/via patterning. However, new resist chemistries or etch methods will need to be deployed for the CD shrink of metal features.

Regardless of which method is employed to provide a CD shrink to single layer DPT patterns, the existence of larger CD shrinks causes problems for DPT layout. This is because CD shrink methods reduce the ability of single exposure processes to pattern small spaces and small pitches. For a given small pitch value, if the aerial image of a feature is made larger, the aerial image of the space to the next features must become smaller. Lithographically there is always a minimum space which can be robustly patterned, so any CD shrink technique will reduce the minimum total feature CD + space value which can be patterned on a single exposure layer. This means that the minimum designed pitch or space value after DPT decomposition will be limited by the amount of CD shrink necessary in the single exposure litho process. The impact of litho CD shrink techniques upon DPT compliance can be observed in Figure 3. From left to right in Figure 3 are different values of litho CD target upsizing, from 0nm to 15nm. This specific example shows the situation for a litho CD increase which will be followed by an etch CD decrease to obtain the final etched wafer CD target, however the problem is identical for the chemical CD shrink method. Also shown in red short lines are the features in the design which are DPT conflicts, that is, are at a space below the minimum resolvable space for a single exposure process. These features will need to be decomposed to different DPT masks. For the upsizing 0nnm case, the layout is easily DPT decomposable. However, as the CD upsizing increases (left to right), it is clear that the number of DPT conflicts to resolve increases rapidly. For the larger upsizing cases, there are so many DPT conflicts that the layout is not DPT decomposable and must be redrawn. Thus it is clear that single exposure DPT lithography will have a significant impact upon the creation of DPT friendly layout.

Another important patterning DPT interaction is the presence of topography on the wafer for the 2nd lithography and etch steps. Figure 4 shows an example of simulation results for a full DPT process flow including topography. Rigorous topographical 3D EMF simulations are performed for lithographic exposures while empirically tuned models are used for deposition and etch steps. Figure 5 shows results of the 2nd lithography step with the same mask and litho conditions but for different underlying topographies. On the left is the resist image with no underlying pattern from the 1st litho/etch steps, and on the right is the resist image with underlying hardmask patterns from the 1st litho/etch steps. Residual ARC non-planarity can also be observed at right. Bottom resist CD measurements show a 2nm or more CD difference due to the impact of the underlying etched patterns in the case at right. This CD difference can not be removed by
3. Mask synthesis implications of double patterning

Accurate and fast DPT decomposition will be needed at the mask synthesis stage. Figure 6 shows an example of standard cell contact patterns after DPT coloring. The green lines (e.g., top-right arrow) indicate single layer space violations which are resolved by DPT. The red lines (e.g., center arrow) indicate layout which cannot be resolved by DPT. Contacts on a routing grid are observed to always be DPT compliant. Off-grid contacts are sometimes non-DPT compliant. Square contacts require only coloring, not cutting. Rectangular contacts often found in SRAM cell layouts do often require cutting. Figure 7 shows an example of decomposed metal lines and the corresponding simulated wafer images. Although the decomposed design intent at top left looks fine, several risky sites can be found in the wafer images at bottom right where critical line-end control is required to ensure overlap or avoid bridging risk. Thus, improvements in single exposure OPC line-end modeling and line-end OPC correction are likely required with DPT. Also required is overlap aware OPC to ensure accurate creation of the combined final etched patterns through process and overlay errors. Figure 8 shows an after-etch simulation of a DPT location in metal with risk of poor overlap which causes an effective pinching error at the intersection of the two individual etch patterns. The final wafer combined pattern can also be seen to have very sharp corners at the overlap location. These sharp corners are not found in single exposure processes. SEM images of DPT patterns (not shown) confirm that these sharp corners exist in DPT etched wafer patterns.

Using the electromagnetic TCAD simulator Raphael™, we investigated whether these sharp corners in DPT layouts are cause for electromigration concern. Figure 9 shows the current density simulation of a hypothetical 22nm node backend copper feature patterned with single exposure. Strong corner rounding on the wafer is observed and the maximum current density is seen to be 1.2 A.U. (arbitrary units). Figure 10 shows the current density simulation of a hypothetical 40nm wide DPT copper feature. There is no corner rounding on wafer (i.e., the corner is square). The maximum current density is seen to be 2.3 A.U., approximately 2X the maximum current density in the single expose case. We then used Black’s equation [3] to estimate the increased risk of electromigration for the square corner case. Using best available estimates of parameter values, the increased risk of electromigration is estimated to be between 3.5X and 4X higher for the square corner case, which is obviously is a cause for concern.

Figure 11 shows vertically mirrored standard cell after a basic and a more complex DPT decomposition. The basic approach runs faster and is less complicated to implement than the complex algorithm but has poorer results, such as DRC errors on a single mask, risky cut locations, more cuts required and asymmetric coloring. The complex algorithm can resolve more DPT conflicts, reduce OPC/yield issues, and provide symmetric output. Figure 12 shows a further example of two different DPT split options of the same layout viewed at the design intent (left) and after etch (right). Split1 uses a rule-based method to analyze the design intent and determine that the circled line-end to line-end overlap region is safe. However, after-etch it is clear the wafer pattern overlap is risky. Split2 uses a more complex model-based analysis to determine that the circled line-end to corner overlap region can be more safely patterned than the line-end to line-end overlap region. Therefore, more complex/intelligent algorithms are seen to significantly improve DPT design and wafer results. However, as DPT methods become more complex, there is more risk disconnect between the DPT check run in design and the decomposition run at mask synthesis. Such a disconnect can lead to a fatal DPT error found only at mask synthesis leading to slow and costly redesign work.

4. Physical design implications of double patterning

Because many layout patterns are not DPT compliant and because finding DPT problems only at mask synthesis is costly, DPT compliant layout must be created at the standard cells, and place & route design stages. Figure 13 shows a flowchart for creation of DPT compliant standard cells. The flow uses a traditional standard cell compaction engine in an iterative loop with a DPT decomposition tool to identify
non-compliant locations. Non-compliant locations are tagged with a rule to fix non-compliance (e.g., add extra space) and are returned to the compactor for fixing. The cycle is repeated until the layout is DPT compliant. Figure 14 shows a sample result of the DPT compliant standard cell generation flow. Three design iterations are shown with the initial 2 DPT errors reduced to 1 DPT error then no DPT errors.

We used the above flow to migrate a set of 70 existing 45nm standard cells created for single exposure patterning to a DPT compliant set. We then compared the total standard cell set area of the two sets. Although we expected that the DPT compliant set would require more area then the original set, the results showed that the DPT compliant set had 1% less area. The reasons for the area shrink appear to be: 1) larger width metal features in a traditional layout require larger than minimum spaces to other features (halation design rules) but not in a DPT layout, 2) the standard cell compaction engine had been improved since the original set of standard cells was created. It is believed therefore that the increase in standard cell area by conversion to DPT compliant cells will be minor. Note that the above work was only for DPT compliance within standard cells, not at their boundaries. We do expect an area increase in placed standard cells but have not yet quantified that impact.

We also evaluated DPT impact upon metal routing. We first analyzed routed metal layers to understand DPT errors in existing 65nm designs. Figure 15 shows an example of common DPT routing errors in routed metals which can be identified with simple design rules (no DPT check required). These errors account for approximately 70% of the total routing DPT errors found and it is believed they can be removed by modifying existing design rules with minimal impact upon routing density or efficiency. Figure 16 shows examples of the remaining approximately 30% of routing DPT errors which cannot be found or resolved by simple design rules. These errors are more complicated and must be identified by a DPT decomposition and error check. A significant number of these complex DPT errors exist in current routing layers. We also modified an existing routing lithography hotspot correction flow in order to test if DPT routing errors could be automatically removed. Figure 17 at left shows an example of a metal2 DPT error (circled) which can be resolved by removing a section of a neighboring metal2 feature and reconnecting (e.g., placing a jumper) on metal4. The image at right shows the placement of landing pads on metal3 layer and vias on via2 layer to connect the metal2 features to the metal4 jumper. Figure 18 at left shows the placement of the jumper on metal4. The right image shows that the targeted DPT error on metal2 is successfully removed. However, it also shows 2 other DPT errors which must still be fixed.

5. Summary and conclusions

In this paper we have explored the interactions between double patterning technology requirements and the lithography patterning, mask synthesis and physical design fields. For lithography, substrate topography and the interactions between pattern shrink and DPT friendly layout were analyzed. For mask synthesis, the benefits of complex decomposition algorithms were noted. However, an increase in algorithm complexity also increases the risk of a layout being certified DPT compliant at the design stage but DPT errors later being found at mask synthesis. For physical design, we developed and tested flows for creating DPT compliant standard cells and metal routing. DPT compliant standard cells appear possible with minimal area penalty, however, DPT compliant metal routing will likely require more area and rework.

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References:
Figure 1. An example of the double litho double etch DPT process which is assumed in this paper. The final wafer image is the superposition of the two lithography images.

Figure 2. Example showing the need for patterning single exposure patterns of etch CD/space ratio of 1/3 with tight control in order to have a final DPT etched 1:1 CD/space ratio.
Figure 3. Metal1 example showing that upsizing the required litho target CD reduces the minimum pitch possible to print with a single exposure and therefore creates more double patterning conflicts in a layout.

Figure 4. Example of simulated process steps in a DPT flow. Rigorous topographical 3D EMF simulations are performed for lithographic exposure. Empirically tuned models are used for deposition and etch.
Figure 5. Example showing substrate topography impact upon the 2nd lithography step. The figure at left has litho2 patterns imaged in a location where there was no layer1 pattern. The profiles are straight and the litho bottom CD is 55nm. The figure at right has litho2 patterns imaged in a location over a layer2 pattern (etch2 pattern visible). The resist profiles are not straight and the litho CD is at least 57nm at the bottom.

Figure 6. Example of standard cell contact patterns after DPT coloring.

Figure 7. Example of decomposed metal lines and the corresponding simulated wafer. Although the decomposed design intent looks fine, several risky sites can be found in the wafer images.

Decomposition must ensure OPC can meet very tight accuracy tolerances - line-end control now critical
Figure 8. After-etch simulation of DPT location in metal with risk of poor overlap. The final wafer combined pattern can also be seen to have very sharp corners at the overlap location.

Figure 9. Current density simulation of a hypothetical 22nm node backend copper feature patterned with single exposure. Strong corner rounding on wafer is observed. The maximum current density is 1.2 A.U.

Figure 10. Current density simulation of a hypothetical 22nm node DPT copper feature. There is no corner rounding on wafer. The maximum current density is 2.3 A.U., ~2X the maximum in single expose case.
Figure 11. Example showing DPT results of mirrored standard cells with a basic algorithm and a more complex algorithm. The basic approach runs faster and is less complicated to implement than the complex algorithm but has poorer results such as DRC errors on a single mask, risky cut locations, more cuts and asymmetric coloring. The complex algorithm can resolve more DPT conflicts (not shown), reduce OPC or yield issues, and provide symmetric output.

Figure 12. Example of two different DPT split options of the same layout viewed at the design intent (left) and after etch (right). Split1 uses a rule-based method to analyze the design intent and determine that the circled line-end to line-end overlap region is safe. However, after-etch it is clear the wafer pattern overlap is risky. Split2 uses a model-based analysis to determine that the circled line-end to corner overlap region can be more safely patterned than line-end to line-end overlap region.
Figure 13. Flowchart showing creation of DPT compliant standard cells. The flow uses a traditional standard cell compactor in an iterative loop with a DPT decomposition tool to identify non-compliant locations. Non-compliant locations are tagged with a rule to fix non-compliance (e.g., add space) and are returned to the compactor for fixing. The cycle is repeated until the layout is DPT compliant.

Figure 14. Sample results of the DPT compliant standard cell generation flow in figure 13. Multiple design iterations are shown with 2 DPT errors reduced to 1 DPT error then zero DPT errors.
Figure 15. Example of common DPT routing errors which can generally be resolved by new design rules.

Simpler odd-cycle DPT hot spots can be automatically detected using rules. Most can be eliminated by slightly modifying the design rules.

This type of error accounts for ~70% of errors in routed metal.

Figure 16. Examples of moderately common DPT errors which cannot be resolved by simple design rules.

Those situations are too complicated for rules to detect.

Must be found using DPT checks.

These can be passed to auto-fix routine for local jumper or rip-up and reroute.

These represent ~30% of errors in layouts analyzed.
Figure 17. Example of metal2 DPT error (circled at left) which can be automatically resolved by removing a section of metal2 and reconnecting (e.g., placing a jumper) on metal4. Right image shows the placement of landing pads on metal3 layer and vias on via2 layer. See also Figure 18.

Figure 18. Example of metal2 DPT error which can be automatically resolved by removing a section of metal2 and reconnecting (e.g., placing a jumper) on metal4. Left image shows the placement of the jumper on metal4. Right image shows that the specific DPT error on metal2 has been removed but that 2 other DPT errors still remain to be fixed. See also Figure 17.